M&M International
AI-Driven Yield enhancement & DX Solutions

Manufacturing × Mathematics × Intelligence

M&M Monthly Letter

Semiconductor Manufacturing & Technology Intelligence

October 2026

Public Edition / Sample Issue

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From Data to Action

Contributing to a sustainable semiconductor industry through technology, data and people.

Prepared by
Takeki Andoh
M&M International

Oct / 2026

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M&M Semiconductor Business Monitor

Oct/2026 (Latest: Aug/2026 Results Basis)

Global Semiconductor Market, Key Applications and Trends
Focus on Image Sensors (Sony) and Analysis of Market, Technology and Business Opportunities.
— Market × Manufacturing × Test × Business —

1 Global Semiconductor Market (Latest: Aug 2026)

Global semiconductor sales reached $82.7B, +3.1% MoM, +21.7% YoY.

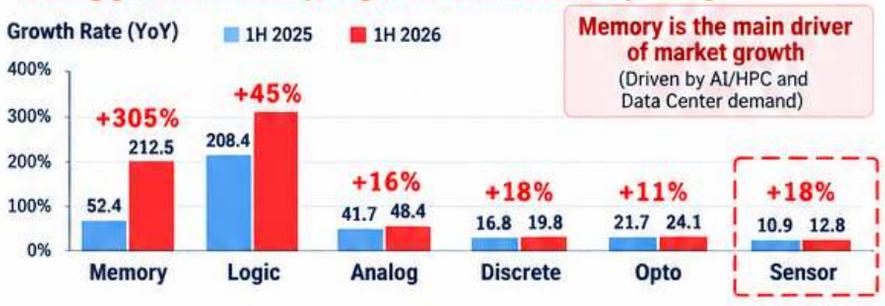


Regional Sales (Aug 2026)

Region	Sales (Billion USD)	MoM	YoY
Total	82.7	+3.1%	+21.7%
Americas	19.5	+4.5%	+33.3%
Europe	4.6	+1.2%	+8.7%
Japan	4.4	+3.5%	+7.9%
Asia Pacific	54.2	+2.7%	+20.1%

2 Product Sales Trends (1H/2026 vs 1H/2025)

Strong growth in memory. Logic and sensors also expanding.



Memory is the main driver of market growth
(Driven by AI/HPC and Data Center demand)

3 Semiconductor Manufacturing & Capex

AI infrastructure drives advanced manufacturing capability and high level of capex.



Q2 2026
$40.53B
+23% YoY
+11% QoQ
(Highest ever in the past 2 years)

300mm Front-End Fab Investment & Capacity (Forecast)

Item	2025	2026 (Forecast)	Growth
Equipment Investment	$11.4B	$14.9B	+31%
Production Capacity (wpm)	8.70M	9.30M	+7%

4 Foundry Market Trends (Q2 2026 Sales & Share)

TSMC maintains ~70% share. Advanced node demand for AI continues.



TSMC	72.5%
Samsung	5.9%
SMIC	5.4%
GlobalFoundries	3.2%
UMC	2.6%
SK hynix System IC	2.3%
HuaHong	1.8%
PSMC	1.6%
VIS	1.4%
Tower	1.2%
Others	4.1%

Key Company Topics (Excerpt)

TSMC	3nm/2nm for AI/HPC strong demand Overseas fab expansion
Samsung	Advanced node investment recovery AI-oriented investment continues
SMIC	Expanding advanced nodes in China Strengthening supply chain resilience
GlobalFoundries	Automotive and industrial demand Stable growth
Rapidus	2nm generation development in Japan Promoting partnerships with global companies (Volume production timing is a key focus)

5 Key Market Drivers

AI and Data Center are the largest growth drivers. Automotive and industrial markets are also recovering.

AI / HPC Data Center

- Growing AI server demand
- Advanced logic and HBM
- Large-scale data center investment

Memory (HBM / DRAM / NAND)

- Rapidly growing HBM demand
- Recovery in DRAM/NAND
- Supply tightness for AI cloud expansion

Smartphone / PC

- Replacement demand for AI-capable devices
- Recovery in inventory adjustment
- Stronger market in 1H 2026

Automotive (xEV / ADAS)

- Electrification and ADAS drive semiconductor demand
- Power semiconductors and sensors
- Recovery in 2H 2026

Industrial / Edge AI

- Factory automation and robotics
- Demand for edge devices
- Expansion of industrial AI
- Increasing digitalization and automation

6 Special Focus — CMOS Image Sensor (CIS) Market Situation and Growth Drivers (Focus on Sony)

CIS Market Size and Growth



CIS market expected to reach $253B in 2025, with further growth toward $280B in 2026.
(Source: Yole Group, 2025 / Compiled by M&M)

Market Share by Major Manufacturers (2025)



Sony's Image Sensor Business (I&SS Segment)

Item	FY2025 (Ended Mar 2026)	YoY
Sales	2,151.5B JPY	+6%
Operating Profit	357.3B JPY	+23%
Image Sensor Sales	1,983.3B JPY	+6%

※ includes smartphone, automotive, and industrial.
※ As-is basis, before business reclassification.
(Source: Sony IR, FY2025 / FY2026 guidance)

Key Applications and Growth Drivers

Smartphone (Mobile)	• Higher resolution / multi-camera • Smaller pixel size • Larger sensor size
Automotive (ADAS / Autonomous)	• More cameras per vehicle • Higher performance and reliability
Industrial (Robot / Inspection)	• Machine vision, inspection • Higher speed / higher sensitivity
Security (Surveillance Infra)	• Higher resolution / lower noise • Wider applications (AI analysis)
New Areas (Spatial AI / XR)	• 3D sensing and depth imaging • New applications for AI devices

M&M VIEW (Image Sensor)

- Sony holds ~50% share, with strong competitiveness in high value-added markets.
- Smartphones are the main driver, followed by automotive and industrial applications.
- Higher resolution, multi-functionality and lower power consumption drive technological innovation.
- Future growth will depend on AI, autonomous driving and XR, with increasing demand for wafer test, probe card and testers.

Key Sources (Public Information)

- WSTS : Global Semiconductor Sales (Aug 2026)
- SEMI : Semiconductor Manufacturing Monitor (Aug/Sep 2026)
- TrendForce : Foundry / Probe Card / Image Sensor Report (2025-2026)
- Sony : Investor Relations (FY2025), Yole Group, and other public information (compiled by M&M)

Prepared by **Takeki Andoh**
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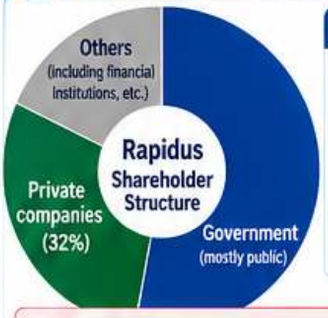
Rapidus Monthly Update
(October 2026)
– Can 2nm Mass Production Be Realized? Business Conditions, Risks, and Future Scenarios –

Key Perspectives from M&M
1. Separate facts and assumptions
2. Focus not only on technology but also on business conditions
3. Consider multiple scenarios for success and potential risks

1 Latest News Highlights (as of October 2026)

Management Update	Rapidus appointed Industry Minister Shinjiro Koizumi as an advisor in August 2026, drawing attention to governance and continuity.	Fact
Progress in 2nm Technology Development	Verification of electrical characteristics using prototype chips (PDK, yield, defect density) is progressing. Production support from TAI systems is also under review.	Fact
Funding and Government Support	Under IPA support, ¥106 billion has already been disbursed. An additional ¥150 billion is expected. The government may establish a maximum ¥1.5 trillion support framework, including conditional share acquisition and preferred shares.	Fact
Customer Engagement	More than 60 companies are in discussions, with about 10 moving to the next stage.	Fact (government material)
Rapidus CORE Development	Cadence, Synopsys, DNP, TOPPAN, Infosys, and Wipro are participating in the 17 partnership projects (Design Solution Associates program).	Fact
Wafer Price Estimate	It is reported that a 300mm wafer may cost ¥3–3.5 million, which is higher than current market prices. The CEO stated that this is not the actual selling price but a preliminary assumption.	Fact
Monthly Fab Plan	A monthly 200,000-wafer fab is targeted around 2040.	Fact (long-term vision)

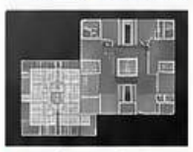
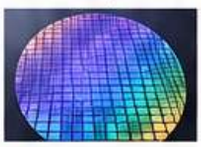
2 Rapidus Shareholder Structure (as of 2026)



Government Ownership Scheme
- **Common shares** (voting rights)
- **Non-voting preferred shares** (to be converted into voting shares if necessary)
- **Golden share** (veto rights on important matters)

Key Points
- Government will monitor management as the largest shareholder
- Private investors are expected to invest after the government establishes a basic framework
- Strict monitoring of capital planning, business plans, and progress

3 Technology Development and Manufacturing Progress (Technology Zone)

2025 (Completed)	2026 (In Progress)	2027 (Target)	2028~ (Next Generation)
2nm GAA Transistor Verification	**PDK Development and Yield Improvement**	**Start of 2nm Mass Production (HVM)**	**1.4nm and Beyond Next Generation Nodes**
			
✓ Verification of electrical characteristics ✓ Test line operation	✓ Customer-oriented PDK ✓ Defect density targets ✓ Verification of TAI system integration	✓ Start of HVM (planned) ✓ Yield, WPH improvement ✓ Changes in production capacity	✓ Evaluation of next-generation devices ✓ Potential capacity expansion

4 Customer Acquisition Status (Business Zone)



Currently Under Discussion (Public information)
- 60+ companies in discussions (government materials)
- ~10 companies in detailed evaluation stage
- Collaboration with Tenstorrent, IBM, and Quest Global, etc.
- First customer PDK release scheduled
- 17 companies participating in Rapidus CORE

Other Important Information (Not yet public)
- Tape-out count / Design WIN count
- Customer name and industry (WSPM)
- 2027 capacity booked WSPM
- Repeat orders
- ASP / gross margin / operating cash flow

5 Investment Payback Estimate (with Annotations)

Basic Model (Educational Estimate)

Total investment (public + private)	~¥5 trillion
Wafer price (2nm, 300mm)	~¥3 million / wafer (assumed cost level)
Investment recovery usage rate	50% (≈ 150,000 wafers/month)
Recovery period	10 years (120 months)

Required wafer production
~28,000 wafers/month
(≈ 1,000 wafers/day)

Required Number of Wafers by Profit Level (per day)

Profit margin (assumed)	Revenue per wafer	Required wafers (per month)	Required wafers (per day)
50%	¥1.5 million	27,800	~930
40%	¥1.2 million	41,600	~1,160
30%	¥0.9 million	55,600	~1,540
20%	¥0.6 million	69,400	~1,930

※ These are simple estimates for educational purposes. Actual values will vary depending on next-generation nodes, yield, cost structure, and R&D expenses.

6 Comparison with Competitors (2nm Generation)

Item	TSMC	Samsung	Rapidus
2nm Mass Production	Q4 2025 (HVM started)	2025–2026 (planned)	2H 2027 (target)
Technology	N2 → N2P/A16	2nm GAA	2nm GAA (IBM technology base)
Key Customers	Apple, NVIDIA, AMD (major)	Mobile, HPC	To be announced (under discussion)
Production Capacity	Large-scale HVM	Large-scale	Initial: medium scale (gradual expansion)
Price (reference)	~$490/wafer (estimated)	Not disclosed	~¥3–3.5 million (reported, may change)

7 Risk Assessment (M&M Evaluation)

Item	Current Evaluation	Comment
Technology Development	△	Progress in 2nm device development, PDK, and yield improvement.
Manufacturing (Mass Production)	△	Actual yield, WPH, and cost per wafer are not yet public.
Customer Acquisition	△	Discussions with 60+ companies. Design WIN and booked WSPM not yet disclosed.
Business Viability	×	Required volume and customer mix unclear. Profitability and operating cash flow remain uncertain.
Governance	△	Government leadership provides stable support, but key personnel changes may affect execution.
External Environment	△	Competition from TSMC/Samsung, geopolitical risks, and macroeconomic uncertainty.

8 Future Scenarios (Stage Gate)

Plan A — 2nm Leading-edge Foundry
- Design WIN (major customer)
- Secure booked WSPM
- Yield and cost competitiveness
- Positive gross margin and operating cash flow

↓ If successful

Plan B — Optimized Manufacturing Architecture
- Single / multi-chamber approach
- Improve batch processing
- Cost reduction and higher WPH

↓ If challenges remain

Plan C — Differentiated Foundry (Pivot to GF model)
- Focus on AI, automotive, communication, and defense
- Chiplet / packaging
- Strategic partnerships
- Specialized markets

9 Conclusion (M&M View)

- ✓ Rapidus is making steady progress in technology development and is moving toward business establishment.
- ✓ However, as a foundry business, Design WIN, booked WSPM, and gross margin visibility are still unclear. The scenario for recovering a ¥5 trillion investment will require stronger external demand.
- ✓ While TSMC and Samsung are ahead in technology and manufacturing, Rapidus has the potential to create strategic differentiation through niche markets and the GF model.
- ✓ It is important to rigorously evaluate Stage Gate milestones, define success criteria for each stage, and maintain the flexibility to revise the strategy.

Technology × Market × Manufacturing × People × Governance
Contributing to a sustainable semiconductor industry through technology, data and people.

Prepared by **Takeki Andoh**
M&M International Oct / 2026

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Human Resources for the AI Era

— From AI Users to Co-creators of New Value —

Developing and Attracting Talent to Create Value Together with AI

Learning from Applied Physics:
How to develop AI-era talent and how companies should respond
Maximize the use of generative AI, foster new value creation, and secure the talent needed to drive next-generation businesses.

1 Key Points of This Article (Author's Message)

1. There are two approaches to AI: a Symbolic AI approach and a Neural Network (Connectionism) approach. It is important to **understand the characteristics of both and use them appropriately.**
2. Generative AI has made significant progress, and the next frontier is **"Spatial AI,"** which can understand and interact with the real world.
3. The required talent is not only users of existing AI, but also people **who can design combinations with new AI** and **apply them to appropriate domains.**
4. An AI agent is an autonomous entity that perceives, thinks, and acts. **It is essential to understand its characteristics and collaborate with it appropriately.**
5. AI-era talent is expected to create new value across a wide range of fields, **including technology, applications, arts, and society.**

2 Two Approaches to AI and Their Characteristics

Symbolic AI (Rule-Based AI)



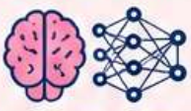
Reasoning through symbols and logic

- Rule-based inference
- Logical and structured processing
- Knowledge representation and combination
- Search and optimization
- Applications in mathematics and physics

Complementary and Integrated Approach

Logic × Data × World Model

Neural Network AI (Connectionism)

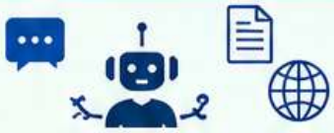


Learning and generation from data

- Learning from images, text, voice, and various data
- Large-scale data-driven learning
- Applications in arts and creative domains
- World simulation (world models)
- Perception and action in physical space

3 From Language AI to Spatial AI — The Next Frontier

Language AI (Current Mainstream)



Large Language Models (LLM)

- Learn language from large-scale text data
- High versatility via the internet
- Strong at grounding to the real world remains limited

Spatial AI (Next Important Domain)



- Understand and interact with the real world
- Applications in robotics, drones, and autonomous systems
- Learning and generation from physical data
- Essential for future industries and society

4 Talent Required in the AI Era

Level 3 AI Orchestrator (Value Creator)		✔ Understand AI characteristics ✔ Design new combinations and create new business ✔ Create social and business value
Level 2 AI Collaborator (Co-creator)		✔ Apply domain expertise and work with AI ✔ Generate results through dialogue with AI ✔ Become a partner for AI in daily work
Level 1 AI User		✔ Use existing AI to improve search, summarization, and content creation ✔ Understand and leverage AI output appropriately

5 Common Misunderstandings and Risks in Adopting AI

✕ Misconceptions (Common Examples)



- ✕ Unclear purpose or evaluation criteria
- ✕ Not verifying the accuracy of output
- ✕ Risk of leakage of technical or confidential information
- ✕ Risk of incorrect output and bias
- ✕ Not leading to new value creation

ⓧ Human × AI Collaboration Process (Recommended)

1. **Define the objective and key questions**
   What do we want to achieve?
2. **Collect information and ask AI**
   Provide the right context and conditions
3. **Verify and deepen the results**
   Verify the output and check sources and logic
4. **Apply domain knowledge and make judgments**
   Combine insights with your own expertise
5. **Summarize and implement**
   Organize the final output and apply it to business

6 Value Created Through Human–AI Co-creation (From a Corporate Perspective)

Acceleration of Technology Development



- Higher efficiency in simulation and analysis
- New idea generation
- Shorter trial-and-error cycles

Improvement of On-site Productivity



- Data analysis and anomaly detection
- Quality improvement and stable operation
- Optimization of equipment and processes

New Business Creation



- New products and services
- Cross-industry collaboration
- Faster response to market changes

Stronger Human Talent and Organizational Capability



- Improved AI literacy
- Integration of domain expertise and AI
- Shift to creative and high-value work

7 My Approach to AI Collaboration (Policy)

— From Manufacturing Experience × AI to Better Conclusions —

Organize On-site Experience (My Assumption)



- Identify key issues from experience
- Formulate hypotheses
- Clarify what you want to know

Collect and Analyze Information with AI (Multi-angle View)



- Organize public information, papers, and data
- Analyze multiple perspectives
- Use charts, calculations, and comparisons

Discussion and Deepening (Expand Thinking)



- Ask questions and get feedback
- Look from different perspectives
- Organize technical, manufacturing, and business viewpoints

Verification and Judgment (Final Decision)



- Evaluate from multiple perspectives
- Assess feasibility, cost, and impact
- Conduct additional investigations if necessary

Documentation and Sharing (Maximize Value)



- Organize into easy-to-understand materials
- Share with colleagues and related departments
- Use as valuable knowledge assets

M&M VIEW (Andoh's Comment)

The value of AI lies not in replacing human work, but in expanding human experience, judgment, and creativity.
Jobs that accept AI output as given tend to decline in value.
Future companies need to develop talent who can use AI to create new value and build organizations that support them.

Source (Original)
Applied Physics, Vol. 95, No. 8 (2026) Special Feature: "Human Resources for the AI Era"
Muneichi Miyake, Tokyo University of Science (and other authors)

Prepared by **Takeki Andoh**
M&M International Oct / 2026

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Quantum Computing: Mechanism, Manufacturing, Measurement, System Operation, and Reliability
– Connecting with Semiconductor Technology (GAA/DC) –

Quantum computing, semiconductors, and they are interconnected.
To understand the quantum era, it is essential to learn the mechanisms, manufacturing, measurement, systems, operation, and reliability. This is the engineering foundation for the future.

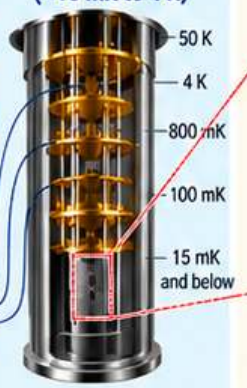
1 Overview of Quantum Computing (QPU)

A quantum computer operates by controlling and measuring quantum bits (qubits) at extremely low temperatures.

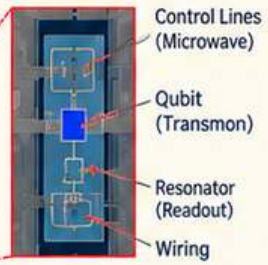
System Components (Control & Measurement)

- Classical Computer (Algorithms & Control Software)
- FPGA / Control Electronics
- DAC (Waveform Generation) ADC (Signal Acquisition)
- RF / Microwave Electronics

Dilution Refrigerator (~10 mK to 4 K)



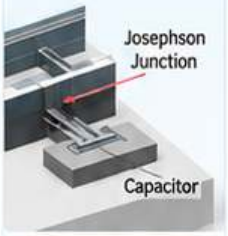
Quantum Chip (QPU) (e.g., Superconducting)



2 Comparison of Major Qubit Platforms

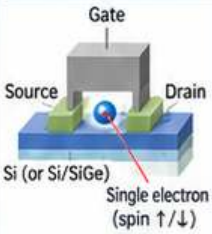
There are multiple approaches to qubits, each with different characteristics and suitable application areas.

Superconducting Qubits (IBM, etc.)



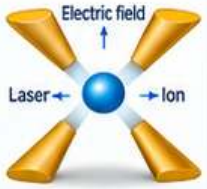
- High-speed operation
- High scalability
- Mature manufacturing process
- Actively used by major companies (IBM, Google, etc.)

Silicon Spin Qubits (Intel, etc.)



- Utilizes CMOS / GAA technology
- Compatible with existing semiconductor processes
- Potential for large-scale integration
- Actively developed by Intel, HRL, etc.

Trapped Ion Qubits

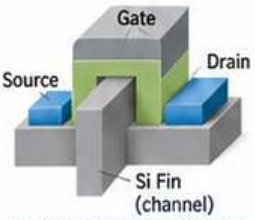


- Extremely high coherence time
- High-precision control and measurement
- Suitable for logical qubits
- Actively developed by Quantinuum, etc.

3 Comparison of Conventional MOSFET (GAA/DC) and Quantum Devices

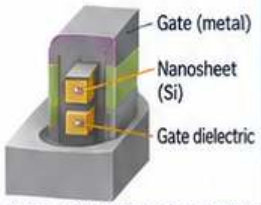
FinFET / GAA technologies used in advanced semiconductor manufacturing are also applied to the fabrication of quantum devices.

Conventional FinFET



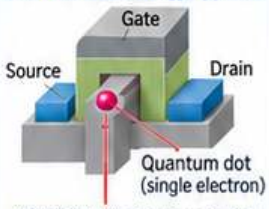
- Multiple electrons controlled
- Vt, Id, leakage, etc. are key evaluation parameters
- High mass production maturity

GAA (DC: Gate-All-Around) (Advanced CMOS)



- Gate controls channel completely
- High current drive capability
- Lower power consumption
- Latest CMOS technology

Silicon/Spin Qubit (GAA/Fin technology applied)

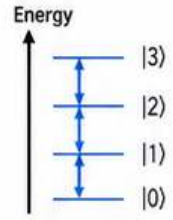


- CMOS/GAA technology applied
- Electron confined in quantum dot
- High compatibility with CMOS manufacturing

4 Why a Josephson Junction Creates 0 and 1

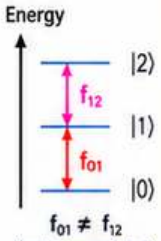
Nonlinear properties allow only two discrete energy states to be selectively controlled.

Energy Levels of Typical LC Circuit



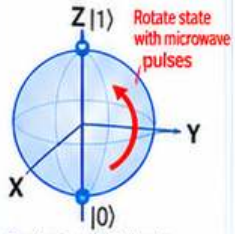
Nearly equally spaced levels

Josephson Junction (Transmon)



$f_{01} \neq f_{12}$ (anharmonicity)

Control with Microwave Pulses

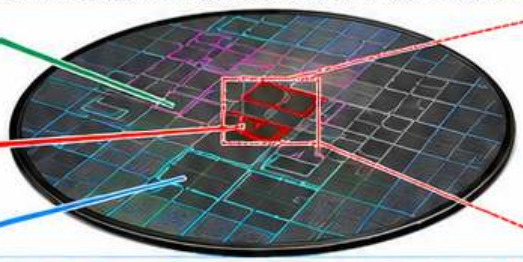


Control qubit state with microwave pulses (Rabi oscillation)

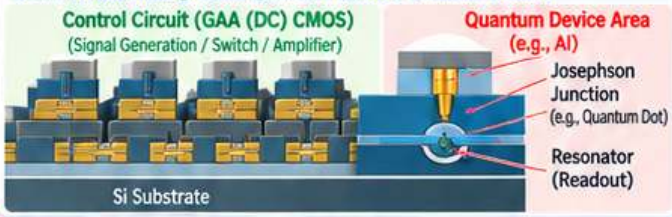
5 Integrated System Concept Combining GAA (DC) and Quantum Devices (Future Vision / Current R&D Stage)

Integrating CMOS (GAA) control circuits with quantum devices to achieve a scalable system is an active research area.

- **GAA (DC) CMOS Control Circuit** (Control / Switch / Amplifier)
- **Quantum Device Area** (Superconducting Qubits / Silicon Spin Qubits)
- **Readout Resonator and Wiring**



Cross-sectional Image (Example: GAA CMOS + Quantum Device)



6 System Architecture (Data Center / Cloud Integration)

A quantum computer is expected to be used in combination with HPC and AI in the future.

Classical Computing Resources (AI / HPC)



- CPU
- GPU
- HPC (large-scale)
- AI models
- Optimization and pre-/post-processing

Hybrid Computing Platform (QURI SDK, etc.)

- Task decomposition (HPC + Quantum)
- Algorithm optimization
- Data processing / Visualization

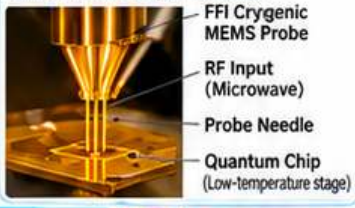
Quantum Computer (Multiple QPU modules)



- QPU Module 1
- QPU Module 2
- ...
- Superconducting QPU
- Silicon Spin QPU
- Others

7 Low-Temperature Measurement and FFI Probe

Insert a MEMS probe into the cryostat to connect to the quantum chip.



8 Manufacturing Flow (Example: Silicon Spin Qubit)

1	Si / SiGe wafer preparation
2	Oxidation and gate dielectric formation
3	Lithography (patterning)
4	Etching and Fin / GAA structure formation
5	Gate / dielectric / contact formation
6	Quantum dot formation
7	Wiring / pad formation
9	Wafer testing (low temperature)
9	Dicing and packaging

9 Operation, Calibration, and Reliability (Current Status and Challenges)

Current Status

- ☑ Qubit parameter measurement (~1 hour per qubit)
- ☑ 1 day calibration cycle
- ☑ Evaluation of T1/T2, gate fidelity, readout error
- ☑ Drift detection and automatic calibration

Main Challenges

- ☑ Gate error (~3 × 10⁻³ level)
- ☑ Readout error
- ☑ Coherence time (T1/T2)
- ☑ Scalability
- ☑ Cross-talk
- ☑ Integration with semiconductor manufacturing processes

Error Correction (QEC) and Key Technologies

- ☑ Logical qubit implemented with multiple physical qubits
- ☑ Error detection, error correction, and syndrome measurement
- ☑ Improvement in coherence time and gate fidelity
- ☑ Large-scale integration and system optimization

10 Technology Maturity and Reliability (Current Status)

Item	Maturity (self-assessment)	Comments
HPC / CPU / GPU	★★★★☆	Highly mature, widely used
Quantum cloud services	★★★☆☆	In practical use (e.g., IBM, etc.)
Single QPU performance	★★☆☆☆	Steady improvement
Quantum error correction (QEC)	★☆☆☆☆	Research and early practical implementation
Large-scale system integration	★☆☆☆☆	In development (target: post-2029)

Quantum computing is currently in the R&D to early engineering stage.
It is already being used in practice, but requires advances in qubit scalability, integration with semiconductor manufacturing, and calibration / error management for full-scale adoption in data center and cloud environments.

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